P/N	SH	REV
610-90631-01	1	1.1

REVISIONS

ECO NO.	REV	DATE	DESCRIPTION	DRAWN	CHECKED	APPROVED
MILI053	1.0	08/30/18	INITIAL RELEASE	ISJP	MILI	MILI
MILI056	1.1	10/17/18	FORMAT UPDATE	ISJP	MILI	MILI

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.
   C. FILL ALL MICROVIAS WITH COPPER PLATING OR NON-CONDUCTIVE EPOXY; DIMPLE DEPTH SHALL BE .025 [.001] MAXIMUM. FOR EPOXY FILL, OVERPLATE WITH COPPER, .005 [.0002] MINIMUM AND THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.
   D. FILL THE THRU VIAS IN PAD USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .005[.0002] MINIMUM THICKNESS. DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

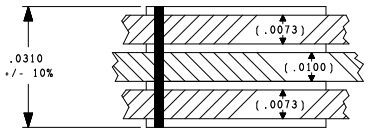
4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR GREEN.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:
   A. FINAL FINISH ON ALL EXPOSED CONDUCTORS SHALL BE IMMERSION SILVER PER IPC-4553, .15 - .38 MICROMETERS [6 - 15 MICROINCHES] THICK.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER	CPW SPACE
L01 - TOP	0.5 OZ	50	.0125	2	-----	---	.-----/.-----	---	-----
L02 - PLANE	0.5 OZ	--	-----	---	-----	---	----	---	-----
L03 - PLANE	0.5 OZ	--	-----	---	-----	---	----	---	-----
L04 - BOTTOM	0.5 OZ	--	.-----	---	-----	---	.-----/.-----	---	-----

STACK-UP (DIMENSIONS IN INCHES)

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS		DATE
DRAWN	Pan Jiang	10/24/18
ENGINEER	Michael Liu	10/24/18
CHECKER	Michael Liu	10/24/18
QA	-	-
PROJ. ENG.	-	-

CYPRESS

TITLE
PCB FABRICATION, CYW920819WCD2

SIZE	CAGE CODE	
D	-	610-90631-01

SCALE	SHEET	REV
1/1	1 OF 2	1.1

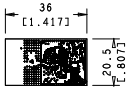
COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

FAB NOTES REV 08/01/14

P/N	SH	REV
610-90631-01	2	1.1

REVISIONS

ECO NO.	REV	DATE	DESCRIPTION	DRAWN	CHECKED	APPROVED
			SEE SHEET 1			



Dimensions are in metric
with inches in brackets.

DRILL CHART: TOP to LO2_GND
ALL UNITS ARE IN MILLIMETERS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	0.1	+0.05/-0.1	PLATED	283

DRILL CHART: LO2_GND to LO3_PWR-GND
ALL UNITS ARE IN MILLIMETERS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	0.15	+0.05/-0.05	PLATED	69

DRILL CHART: LO3_PWR-GND to BOTTOM
ALL UNITS ARE IN MILLIMETERS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	0.1	+0.05/-0.1	PLATED	38

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILLIMETERS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	0.15	+0.05/-0.05	PLATED	197
·	0.381	+0.05/-0.05	PLATED	146
•	0.762	+0.0762/-0.0762	NON-PLATED	2
•	1.016	+0.0762/-0.0762	NON-PLATED	2

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SIZE	CAGE CODE	610-90631-01	
D	_		
SCALE 1/1		SHEET 2	REV 1.1

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